LONTIUM SEMICONDUCTOR CORPORATION

ClearEdge™ Technology

LT8911EXB

MIPI® DSI/CSI Bridge to eDP

Datasheet

1. Features

- **Single-Port MIPI® DSI Receiver**
  - Compliant with D-PHY1.2, DSI1.3 and CSI1.3
  - 1 clock lane and 1~4 configurable data lanes
  - 80Mb/s~2.0Gb/s per data lane
  - Data lane and polarity swapping
  - Data lane input de-skew
  - Internal Rterm calibration w/i less than 5% error
  - 3-bit programmable equalization
  - Support Burst and Non-Burst Mode
  - Support 16/18/24/30/36-bit RGB and YUV format
- **eDP1.4 Transmitter**
  - Compliant to VESA eDP1.4 standard
  - Support1/2/4 data lanes with 1.62Gbps(RBR) or 2.7Gbps(HBR).
  - Data lane and polarity swapping
  - Optional SSC 0.5% down-spreading output
  - Configurable and power-on-calibrated output swing for optimized EMI
  - Support PWM Backlight control
  - MCCS over AUX channel
- **Miscellaneous**
  - Single 1.8V supply power
  - Temperature range: −40°C to +85°C
  - Packaged in 6mm x 6mm QFN48

2. General Description

The Lontium LT8911EXB MIPI®DSI/CSI to eDP converter features a single-port MIPI receiver with 1 clock lane and 4 data lanes operating at maximum 2.0Gbps per data lane; a maximum input bandwidth of 8.0Gbps. The converter decodes the input MIPI® DSI 16/18/24/30/36-bit RGB packets and converts the formatted video data stream to a single-link VESA eDP1.4 compliant output with 1/2/4configurable data lanes, supporting RBR(1.62Gbps) and HBR(2.7Gbps) link speeds. The build-in optional SSC function reduces EMI effect on EMI-concerned system application.

The LT8911EXB are fabricated in advanced CMOS process and implemented in a small outline 6mm x 6mm QFN48 at 0.5mm pitch package respectively. This package is RoHS compliant and specified to operate from −40°C to +85°C.

3. Applications

- Mobile systems
- Cellular handsets
- Digital video cameras
- Digital still cameras
- Personal media players
- Gaming

Figure 3.1 Application Diagram

4. Ordering Information

Table 4.1 Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
LT8911EXB	−40° C to +85° C	QFN48 (6*6)	Tray

Lontium Semiconductor

Table of Contents

5. Revision History

Version	Owner	Content	Date
R1.0	XY J	Initial Release	24/11/2017
	N W	Update package information	27/12/2017

6. Pinning Information

6.1 Pin Configuration

To improve signal integrity, all differential pairs should be routed with 100Ω±10% differential impedance.Maximum trace length mismatch should be less than 5mil and keep total trace length to a minimum for all differential traces. Routing differential pairs on the top or bottom layer with no vias as on signal path is highly recommended.

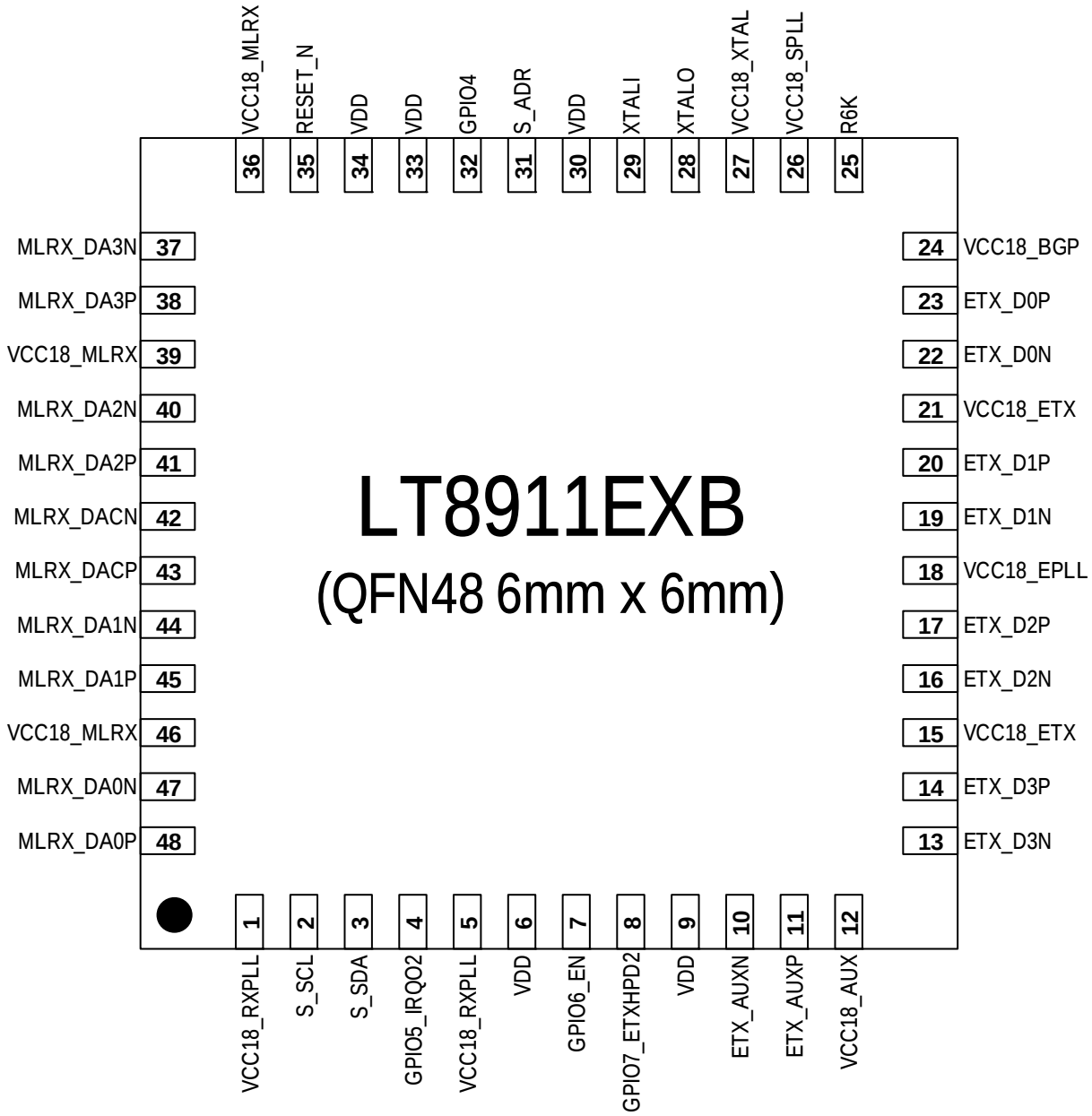


Figure 6.1.1 LT8911EXB Pin Assignment (Top View)

For crystal oscillator, keep XTALI/XTALO as short as possible and away from noisy signal source. Minimize parasitic capacitances on these two pins and shield them with clean ground lines.
To minimize the power supply noise floor, at least one 0.1μF and one 0.01μF decoupling capacitoris recommended to be installed near all the LT8911EXB 1.8V power pins. To avoid large current loops and trace inductance, thetrace length between decoupling capacitor and device power inputs pins must be minimized.

6.2 Pin Description

Table 6.2.1 Pin Description

Pin No.	Pin Name	Description
1	VCC18_RXPLL	**RXPLL 1.8V Power** 1.8V power for RXPLL
2	S_SCL	**I2C Data Clock** It serves as the serial port data clock slave for register access. Supports 1.8V CMOS logic.
3	S_SDA	**I2C Data IO** It serves as the serial port data IO slave for register access. Supports 1.8V CMOS logic.
4	GPIO5_IRQO2	**Interrupt Request Output** In default, this pin is configured as interrupt request (IRQ) output. **Digital Test Signal Output** When this pin is configured as GPIO, it serves as digital test signal output.
5	VCC18_RXPLL	**RXPLL 1.8V Power** 1.8V power for RXPLL
6	VDD	**Digital core 1.8V Power** 1.8V power for digital core
7	GPIO6_EN	**ChipEnable (High Active)** In default, this pin is configured as chip enableinput. **Digital Test Signal Output** When this pin is configured as GPIO, it serves as digital test signal output.
8	GPIO7_ETXHPD2	**eDPTx HPD Control** In default, this pin is configured as eDPTX hot-plug detectinput. **Digital Test Signal Output** When this pin is configured as GPIO, it serves as digital test signal output.
9	VDD	**Digital core 1.8V Power** 1.8V power for digital core
10	ETX_AUXN	**eDPTx AUX Channel Negative Output**
11	ETX_AUXP	**eDPTx AUX ChannelPositive Output**
12	VCC18_AUX	**eDPTx AUX Channel Power** 1.8V power for eDP AUX channel
13	ETX_D3N	**eDPTxPHY Port-A Data Lane-3 Negative Output** eDPTx output data up to 2.7Gb/s.
14	ETX_D3P	**eDPTxPHY Port-A Data Lane-3 Positive Output** eDPTx output data up to 2.7Gb/s.
15	VCC18_ETX	**eDPTx PHY 1.8V Power** 1.8V power for eDPTxPHY
16	ETX_D2N	**eDPTxPHY Port-A Data Lane-2 Negative Output** eDPTx output data up to 2.7 Gb/s.
17	ETX_D2P	**eDPTxPHY Port-A Data Lane-2 Positive Output** eDPTx output data up to 2.7Gb/s.
18	VCC18_EPLL	**eDPTxPLL1.8V Power** 1.8V power for eDPTx PLL
19	ETX_D1N	**eDPTxPHY Port-A Data Lane-1 Negative Output** eDPTx output data up to 2.7Gb/s.
20	ETX_D1P	**eDPTxPHY Port-A Data Lane-1 Positive Output** eDPTx output data up to 2.7Gb/s.
21	VCC18_ETX	**eDPTx PHY 1.8V Power** 1.8V power for eDPTxPHY
22	ETX_D0N	**eDPTxPHY Port-A Data Lane-0 Negative Output** eDPTx output data up to 2.7Gb/s.
23	ETX_D0P	**eDPTxPHY Port-A Data Lane-0 Positive Output** eDPTx output data up to 2.7Gb/s.
24	VCC18_BGP	**Bandgap1.8V Power** 1.8V power for bandgap
25	R6K	**BandGap External Resistor** External 6K resistor for setting internal reference current.
26	VCC18_SPLL	**SYSPLL 1.8V Power** 1.8V power for System PLL

Pin No.	Pin Name	Description
27	VCC18_XTAL	**Crystal IO 1.8V Power** 1.8V power for Crystal IO
28	XTALO	**Crystal Clock Output** A crystal oscillator should be attached between this pin and XTALI. If XTALI is used as reference clock input, this pin must be floating.
29	XTALI	**Crystal Clock Input** A crystal oscillator should be attached between this pin and XTALO. However, a CMOS 1.8V compatible clock signal can also be connected to this pin as reference clock of LT8922
30	VDD	**Digital core 1.8V Power** 1.8V power for digital core
31	S_ADR	**I2C Device Address Select** It serves as the serial port address select. Supports 1.8V CMOS logic.
32	GPIO4	**Digital Test Signal Output** When this pin is configured as GPIO, it serves as digital test signal output.
33	VDD	**Digital core 1.8V Power** 1.8V power for digital core
34	VDD	**Digital core 1.8V Power** 1.8V power for digital core
35	RESET_N	**Hardware Reset Input** Chip reset signal. Active LOW.
36	VCC18_MLRX	**MIPI® D-PHY PHY Power** 1.8V power for MLRX
37	MLRX_DA3N	**MIPI® D-PHY Port-A Data Lane-3 Negative Input** Negative input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s.
38	MLRX_DA3P	**MIPI® D-PHY Port-A Data Lane-3 Positive Input** Positive input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s.
39	VCC18_MLRX	**MIPI® D-PHY Power** 1.8V power for MLRX
40	MLRX_DA2N	**MIPI® D-PHY Port-A Data Lane-2 Negative Input** Negative input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s.
41	MLRX_DA2P	**MIPI® D-PHY Port-A Data Lane-2 Positive Input** Positive input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s.
42	MLRX_DACN	**MIPI® D-PHY Port-A Data Clock Lane Negative Input** Negative input of DDR clock differential pairs up to 750Mb/s in quadrature phase with data signals.
43	MLRX_DACP	**MIPI® D-PHY Port-A Data Clock Lane Positive Input** Positive input of DDR clock differential pairs up to 750Mb/s in quadrature phase with data signals.
44	MLRX_DA1N	**MIPI® D-PHY Port-A Data Lane-1 Negative Input** Negative input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s.
45	MLRX_DA1P	**MIPI® D-PHY Port-A Data Lane-1 Positive Input** Positive input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s.
46	VCC18_MLRX	**MIPI® D-PHY Power** 1.8V power for MLRX
47	MLRX_DA0N	**MIPI® D-PHY Port-A Data Lane-0 Negative Input** Negative input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s.
48	MLRX_DA0P	**MIPI® D-PHY Port-A Data Lane-0 Positive Input** Positive input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s.

7. Function Block Diagram

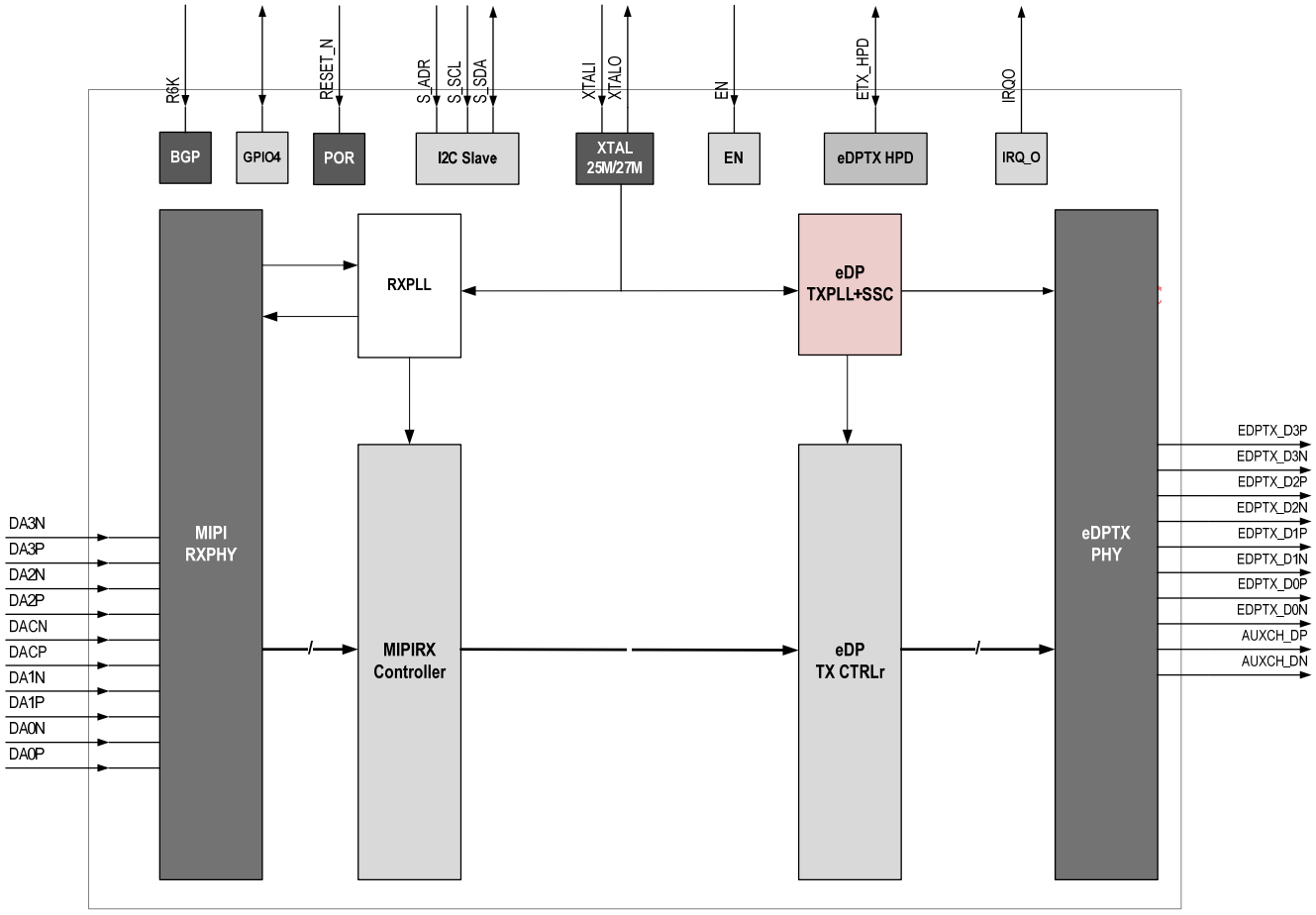


Figure 7.1 Function Block Diagram

8. Electrical Characteristics

8.1 Absolute Maximum Conditions

Table 8.1.1 Absolute Maximum Conditions

Symbol	Description	Min	Typ	Max	Unit
VCC18_MLRX, VCC18_ETX VCC18_SPLL, VCC18_XTAL VCC18_BGP, VDD	1.8V Power Supplay Voltage	-0.3		2.0	V
V_I	CMOS Terminal Input Voltage Range	-0.3		2.0	V
V_O	CMOS Terminal Output Voltage Range	-0.3		2.0	V
T_S	Storage Temperature	-55		125	℃
ESD	HBM Elastrostatic Discharge Level			TBD	V

Notes:
1.Permanent device damage may occur if absolute maximum conditions are exceeded.
2.Function operation should be restricted to the conditions described under Normal Operating Conditions.

8.2 Normal Operating Conditions

Table 8.2.1 Normal Operating Conditions

Symbol	Description	Min	Typ	Max	Unit
	1.8V Power Supplay Voltage	1.62	1.8	1.98	V
VCC_N	Power Supply Voltage Noise			50	mV
T_A	Operating Free-air Temperature	-40	27	85	℃

8.3 DC Characteristics

Table 8.3.1 DC Characteristics

MIPI HS Line Receiver DC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
VIDTH	Differential input high voltage threshold			70	mV
VIDTL	Differential input low voltage threshold	-70			mV
VIHHS	Single ended input high voltage			460	mV
VILHS	Single ended input low voltage	-40			mV
VCMRXDC	Input common mode voltage	70		330	mV
	Differential input impedance	80		125	Ω
MIPI LP Line Receiver DC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
VIL-ULPS	Logic 0 input voltage, in ULP State			300	mV
VIL	Logic 0 input voltage, not in ULP State			550	mV
VIH	Input high voltage	880			mV
VHYST	Input hysteresis	25			mV
MIPI Contention Line Receiver DC Specifications					

Symbol	Parameter	Min	Typ	Max	Unit
VILF	Input low fault threshold	200		450	mV
eDP Transmitter DC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
Vbias_TX	TX DC Bias Voltage	0		2	V
Vtx_ac_cm_hbr2	TX AC Common Mode Voltage			20	mV rms
Vtx_ac_cm_hbr2	TX AC Common Mode Voltage			30	mV rms
Vtx_diff_vpp_level0	Differential Peak to Peak Output Swing Level0	0.34	0.4	0.46	V
Vtx_diff_vpp_level1	Differential Peak to Peak Output Swing Level1	0.51	0.6	0.68	V
Vtx_diff_vpp_level2	Differential Peak to Peak Output Swing Level2	0.69	0.8	0.92	V
Vtx_pre_emp_ratio	Pre-emphasis level 0	0	0	0	dB
	Pre-emphasis level 1	2.8	3.5	4.2	dB
	Pre-emphasis level 2	4.8	6	7.2	dB
	Pre-emphasis level 3	7.5	9.5	11.4	dB
Ctx	AC couple capacitance	75		200	nF
TX_SHORT	TX short circuit current limit			50	mA
RTX_DIFF	Differential Impedance	80	100	120	Ω

8.4 AC Characteristics

Table 8.4.1 AC Characteristics

MIPI HS Line Receiver AC Specifications

Symbol	Parameter	Min	Typ	Max	Unit
ΔVCMRX(HF)	Common mode interference beyond 450MHz			200	mVpp
ΔVCMRX(LF)	Common mode interference between 50MHz and 450MHz.	-50		50	mVpp
Ccm	Common mode termination			60	pF
Rterm	Termination Resister	80	100	125	Ω
MIPI LP Line Receiver AC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
eSPIKE	Input pulse rejection			300	V.ps
TMIN	Minimum pulse response	20			ns
VINT	Peak interference voltage			200	mV
fINT	Interference frequency	450			MHz
eDP Transmitter AC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
Ttx_eye_chip_HBR	Minimum TX eye width at pkg pin	0.72			UI
Ttx_jitter_HBR	Maximum time between the jitter median and maximum				
	deviation from the median at TX pkg pin			0.147	UI
Ttx_eye_chip_RBR	Minimum TX eye width at pkg pin	0.82			UI
Ttx_jitter_RBR	Maximum time between the jitter median and maximum deviation from the median at TX pkg pin			0.09	UI

Ttx_rise_chip Ttx_fall_chip	D+/D- TX output rise and fall time at TX pkg pins	50		130	ps
RL_TX_DIFF	Differential Return Loss at 0.675Ghz at TX pkg pins	12			dB
	Differential Return Loss at 1.35Ghz at TX pkg pins	9			dB
Ttx_skew	Lane intra pair output skew at pkg pins			20	ps
Ttx_rise_fall	Lane intra pair rise and fall time mismatch at pkg ins			5	%

8.5 Power Consumption

Table 8.5.1 Power Consumption

Resolution	Input	Output	Power Consumption (mA)
1366x768	2-Lane MIPI	1-Lane/2.7G/Level3	TAB
	3-Lane MIPI		
	4-Lane MIPI		
1080P	4-Lane MIPI	2-Lane/2.7G/Level3	

9. Hardware Implementation

- MLRX_DA*P/N and MLRX_DB*P/N pairs should be routed with controlled 100Ω differential impedance (±10%) or 50Ω

- Intra-pair skew should be kept as small as possible and It is recommended to keep lengths to within 5 mils of each other.
- Length matching should be near the location of mismatch.
- Each pair should be separated at least by 3 times the signal trace width and Keep away from other high-speed signals.
- The use of bends in differential traces should be kept to a minimum. When bends are used, the number of left and right bends should be as equal as possible and the angle of the bend should be ≥ 135º. This will minimize any length mismatch caused by the bends and therefore minimize the impact bends have on EMI.
- Route all differential pairs on the same layer and Do not route differential pairs over any plane split.
- The number of VIAS should be kept to a minimum. Keeping the VIAS count to 2 or less is recommended.
- Keep traces on layers adjacent to the ground plane.
- Adding test points will cause impedance discontinuity, therefore, negatively impacting signal performance. If test points are used, they should be placed in series and symmetrically. They must not be placed in a manner that causes a stub on the

- The maximum trace length over FR4 betweenLT8911EXB and MIPI signal source is 25~30 cm.

9.2 Embedded DisplayPort Interface

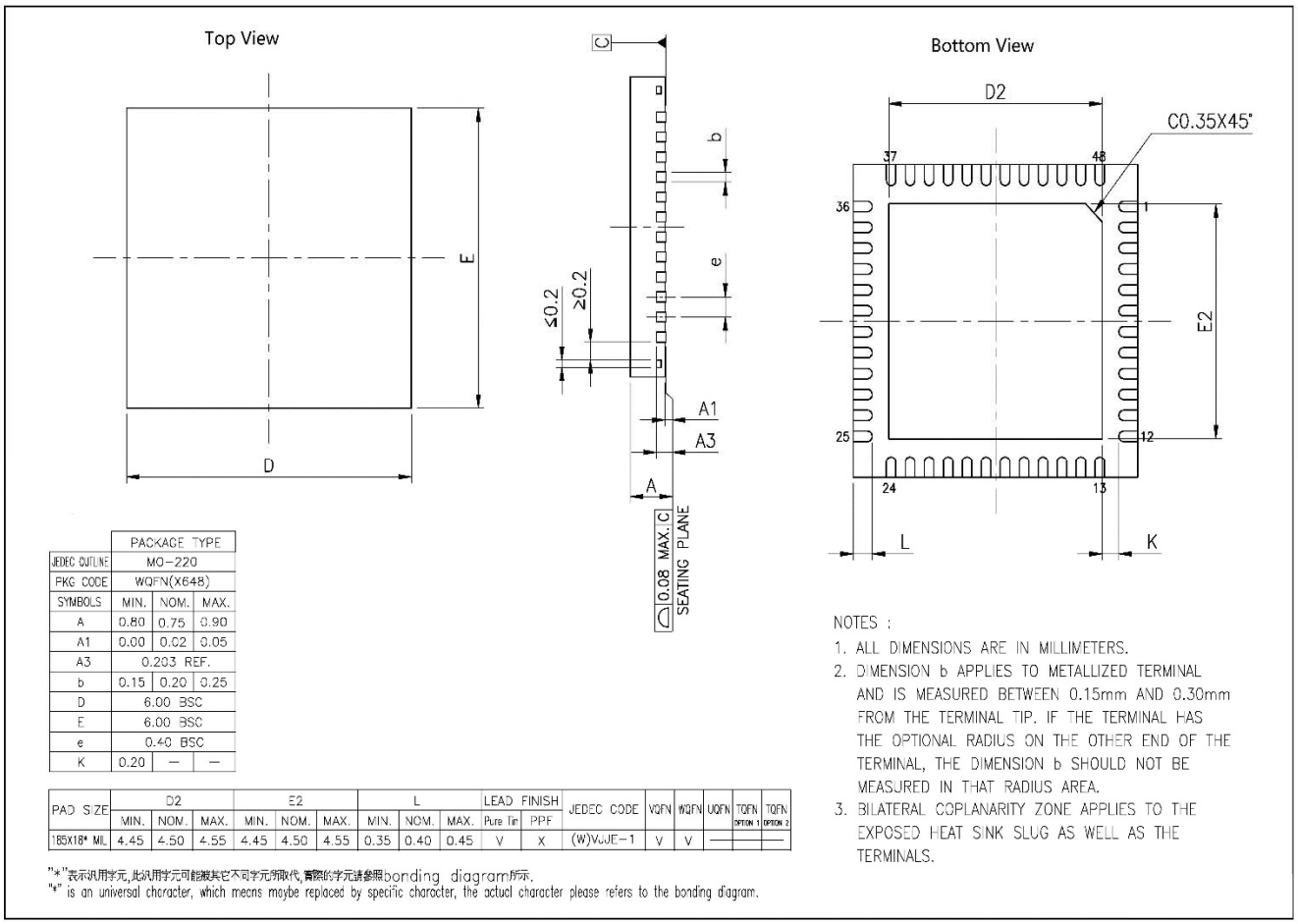
All eDPTX pins require AC coupling capacitors between the LT8911EXB and the eDPsink. It is recommended these capacitors are placed close to the eDP receptacle. The AC coupling capacitor must be in the range of 75nF to 200nF. A value of 100nF is recommended. A package size of 0201 is recommended but a 0402 is acceptable.

- ETX_D*P/N and ETX_AUXP/N pairs should be routed with controlled 100Ω differential impedance (±10%) or 50Ω single-ended impedance (±8%).
- Intra-pair skew should be kept as small as possible. It is recommended to keep lengths to within 5 mils of each other.
- Length matching should be near the location of mismatch.
- Each pair should be separated by at least 3 times the signal trace width and Keep away from other high-speed signals.
- The use of bends in differential traces should be kept to a minimum. When bends are used, the number of left and right bends should be as equal as possible and the angle of the bend should be ≥ 135º. This will minimize any length mismatch caused by the bends, therefore, minimizing the impact bends have on EMI.
- Route all differential pairs on the same layer and Do not route differential pairs over any plane split.
- The number of VIAS should be kept to a minimum. Keeping the VIAS count to 2 or less is recommended.
- Keep traces on layers adjacent to the ground plane.
- Adding test points will cause impedance discontinuity, therefore, negatively impacting signal performance. If test points are used, they should be placed in series and symmetrically. They must not be placed in a manner that causes a stub on the differential pair.
- The maximum trace length over FR4 between LT8911EXB and the eDP receptacle is 4 inches for data rates ≤ HBR (2.7 Gbps).
-

9.3 Clock

10. Package Information

The LT8911EXB is available in QFN48 6mm x 6mm package with exposed pad (E-PAD 4.5*4.5). E-PAD incorporates features that provide a very low thermal resistance path for heat removal from the IC. The E-PAD on the device must be soldered to the PCB ground plane for proper electrical and thermal performance.



	PACKAGE TYPE		
JEDEC OUTLINE	MO-220		
PKG CODE	WQFN(X648)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.75	0.90
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	6.00 BSC		
E	6.00 BSC		
e	0.40 BSC		
K	0.20	—	—

PAD SIZE	D2			E2			L			LEAD FINISH		JEDEC CODE	VQFN	WQFN	UQFN	TQFN OPTION 1	TQFN OPTION 2
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF						
185X18* MIL	4.45	4.50	4.55	4.45	4.50	4.55	0.35	0.40	0.45	V	X	(W)VJJE-1	V	V	—	—	—

"*"表示讯用字元,此讯用字元可能被其它不同字元所取代,實際的字元請參照bonding diagram所示.
"*" is an universal character, which means maybe replaced by specific character, the actual character please refers to the bonding diagram.

Figure 10.1 LT8911EXB QFN486mmx6mm Package

Visit our corporate web page at: www.lontiumsemi.com
Technical support: support@lontium.com
Sales: sales@lontium.com